Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**NOTE: PIN ASSIGNMENT NOT CONFIRMED**

**PAD FUNCTION:**

1. **VOUT**
2. **+IN**
3. **–IN**
4. **BIPOLAR OFFSET CURRENT**
5. **–VS**
6. **ONE-SHOT CAPACITOR**
7. **NC**
8. **FOUTPUT**
9. **COMPARATOR INPUT**
10. **DIGITAL GND**
11. **ANALOG GND**
12. **+VS**
13. **OFFSET NULL**
14. **OFFSET NULL**

**.088”**

**AD650**

**MASK**

**REF**

**1**

**14**

**13**

**2 3**

**4**

**5**

**6**

**8 9 10 11 12**

**.090”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential:**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .087” X .090” DATE: 11/25/20**

**MFG: ANALOG DEVICES THICKNESS .019” P/N: AD650K**

**DG 10.1.2**

#### Rev B, 7/1